



# Europa Orbiter/X2000 Avionics Industry Briefing



## Europa/X2000 Avionics Overview

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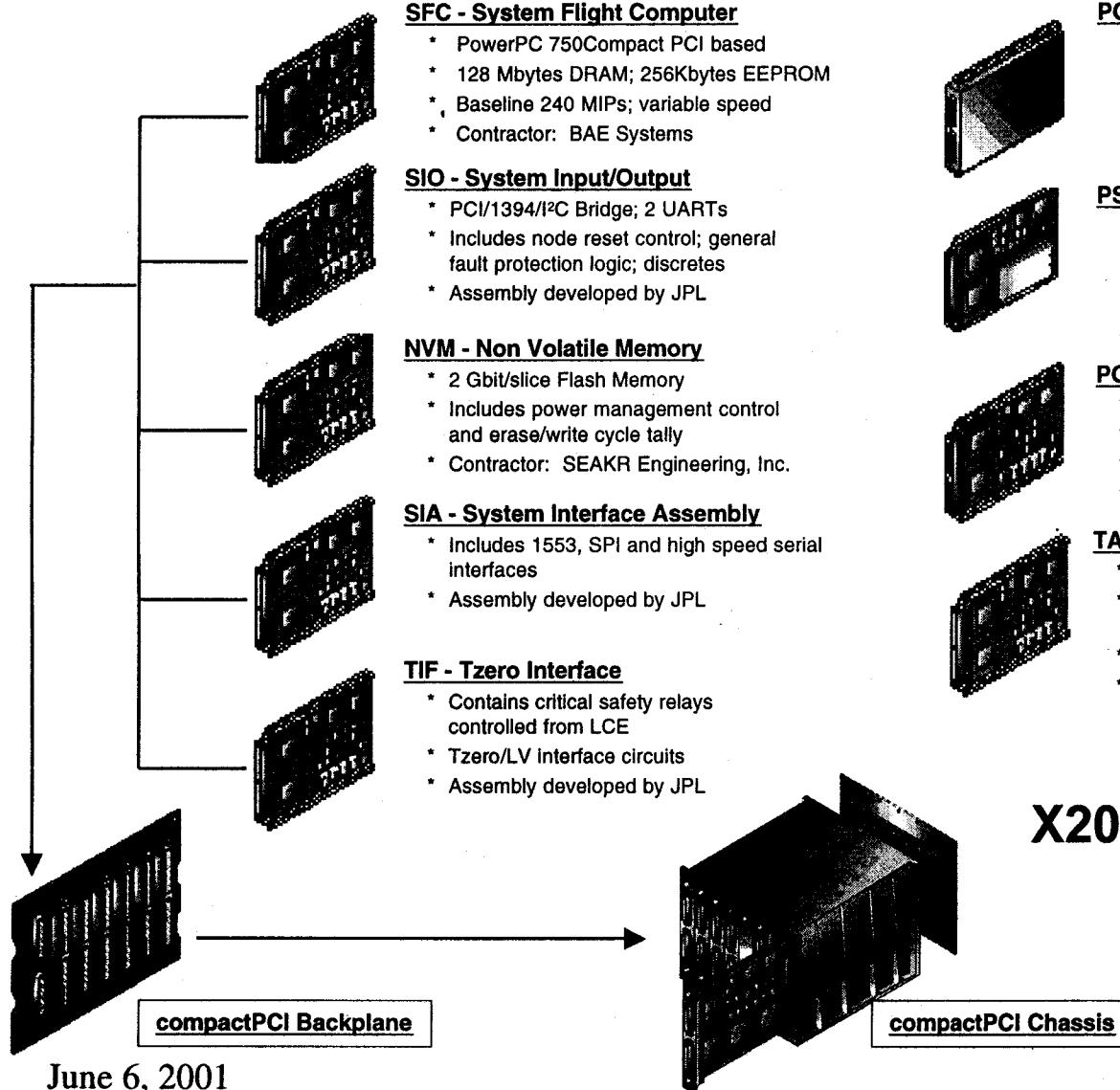
June 6, 2001



## Key Technologies/Driving Requirements

- Next generation spacecraft microprocessor technology
- Open architecture for advanced spacecraft systems based on commercial interfaces
- Advanced digital ASIC technology (SOI, HX3000, 1 M gates)
- Low voltage, low power system architectures
- Advanced power management and control
- Next generation Power Activation and Switching Module (PASM)
- Advanced high efficiency power converter
- Advanced mixed signal ASIC technology (SOI, HX2000)
- 1 Mrad radiation requirement
- New, low-cost approach to avionics system development using commercial IP
- Initiating first step towards System on a Chip for future missions
- Fault tolerant tree topology using IEEE-1394a (Firewire) bus
- Low power, fault tolerant I<sup>2</sup>C serial bus
- compactPCI 3U form factor packaging approach

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## PCA - Power Converter Assembly

- \* Two 30 W primary to secondary Power Converter Modules (PCMs) on 1 slice
- \* Two versions: dual 3.3V PCMs or one 3.3V and one 5V PCM
- \* Contractor: Lockheed Martin CSS

## PSS - Power Switch Slice

- \* Used to switch power loads, valves and pyros (all three functions)
- \* 16 switches/slice
- \* Redundant I<sup>2</sup>C bus
- \* Contractor: Lockheed Martin CSS

## PCS - Power Control Slice

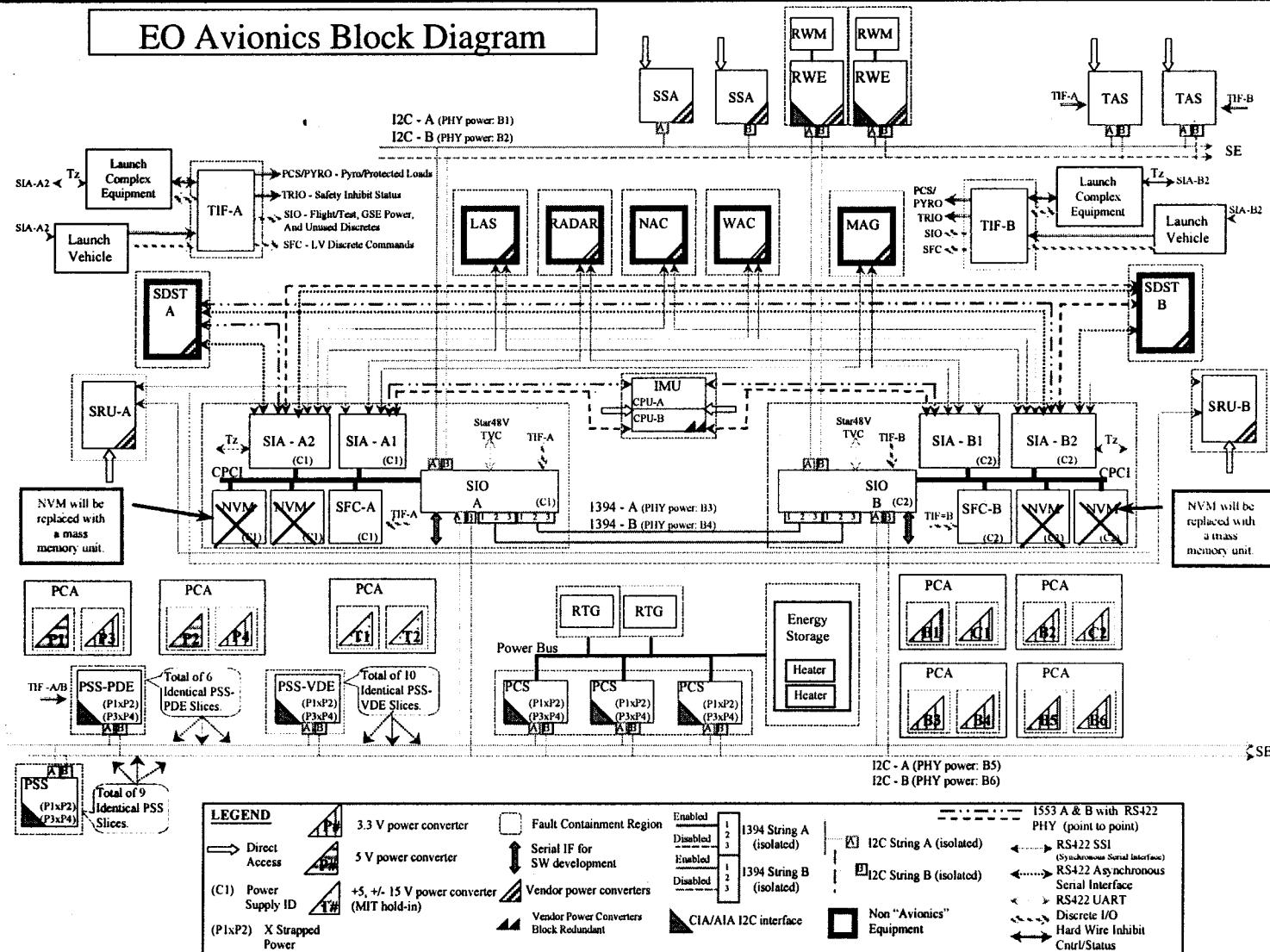
- \* Primary spacecraft power bus regulation
- \* Includes shunt regulator control
- \* Redundant I<sup>2</sup>C bus
- \* Contractor: Lockheed Martin CSS

## TAS - TRIO Assembly Slice

- \* Temperature and analog collection
- \* 6 Temperature Remote I/O (TRIO) ASICs split between 2 I<sup>2</sup>C buses
- \* 96 telemetry channels; 10 bit A/D
- \* Contractor: Johns Hopkins University/Applied Physics Laboratory

## X2000 Avionics Hardware

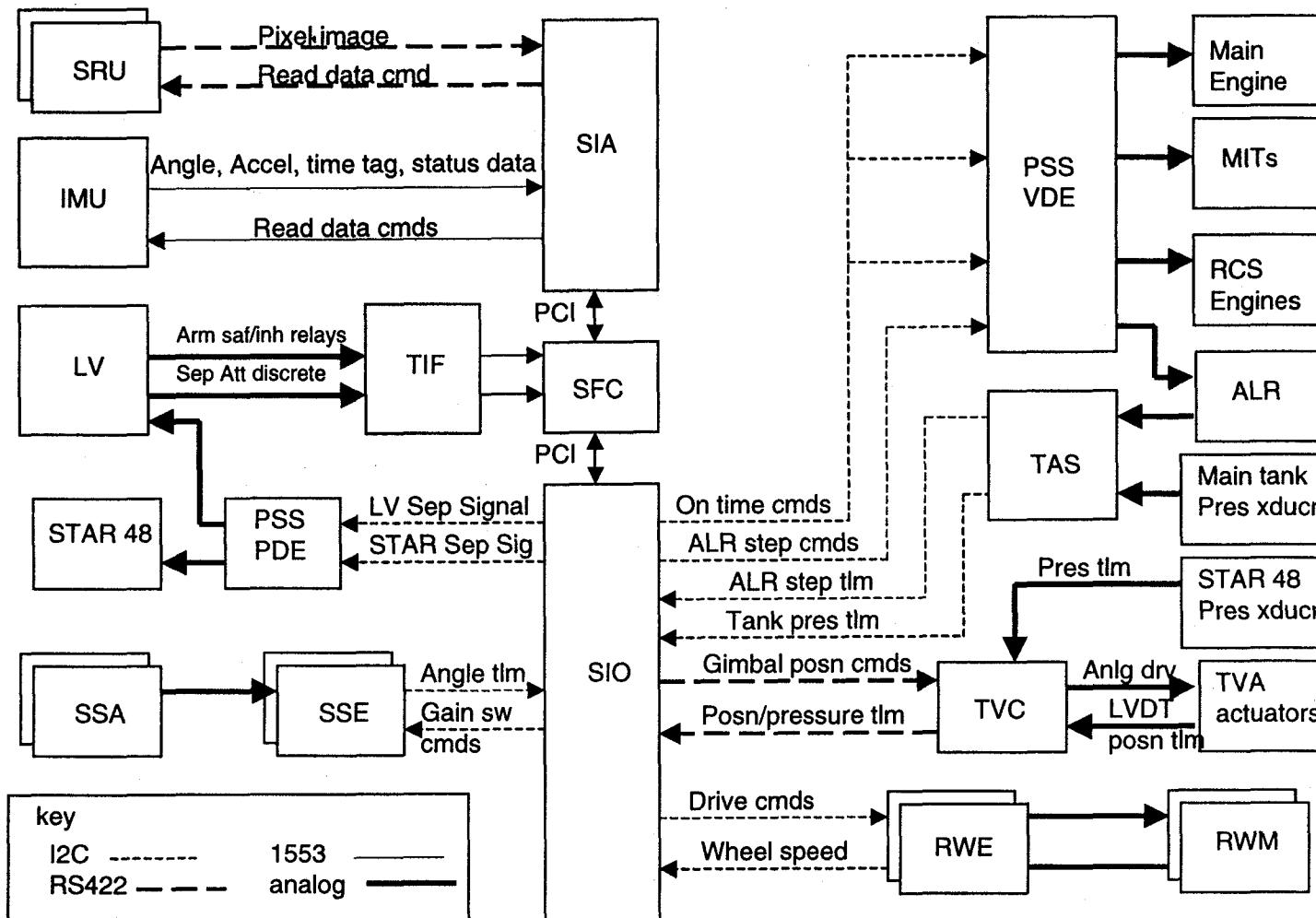
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## EO ACS/Avionics Functional Block Diagram





## Command & Data Handling Subsystem ASICs

	ASIC	Function	Slice	Designed By	Proc By	Fab By	Fab Line Type	Gate Count	Pin Count	Status
1	Power PCI Bridge Chip	Bridge between the Compact PCI (cPCI) bus, memory (EEPROM, SDRAM) and the RAD750 processor. Includes UART and JTAG interfaces for software support and diagnostics.	SFC	BAE	BAE	BAE	Digital	700K	624	First fab run completed. Parts installed on EM SFCs currently going through qualification. (Enhanced Bridge Chip = 200 Krad)
2	RAD750	Rad hard version of the PowerPC 750 processor.	SFC	BAE	BAE	BAE	Digital	10M Transistors	360	First fab un completed 5/01. Parts in test.
3	DIO (Digital I/O)	Bridge between the 1394/I <sup>2</sup> C buses and the cPCI bus. Implements the link layer of the 1394 bus, the two I <sup>2</sup> C bus controllers, and logic for fault tolerance enhancements. Includes a UART to support software development and discrete I/O signals for miscella	SIO	JPL + Mentor/ISI	JPL	Honeywell SSEC	Gate Array HX311G	170K gates + 250KB RAM	220 Sig 100 Pwr	FPGA version in checkout. PDR date: 6/27/01
4	MSIO (Mixed Signal I/O)	Implements the physical layer of the 1394 bus and the drivers of the I <sup>2</sup> C buses.	SIO	SSEC/DMC + Mentor/ISI + JPL	JPL	Honeywell SSEC	Mixed Signal HX2300	50K gates + analog 1394 I/f	200 Sig 150 Pwr	CDR completed 5/18/01
5	SIA (System Interface ASIC)	Provides interface between the cPCI bus, the 1553 bus controller ASIC, buffer memory (SRAM), SDST (RS422) and 4 high speed serial interfaces (instruments/sensors).	SIA	JPL + Asgard ASIC	JPL	Honeywell SSEC	Digital HX311G			FPGA version in checkout. PDR date: 11/01
6	Memory Controller ASIC	Interface between cPCI bus and memory (flash). Includes Reed Solomon EDAC and flash power control.	NVM	SEAKR	SEAKR	Honeywell SSEC	Digital HX2160	~70K		ASIC in fabrication. PODs received 5/30 and in checkout. (300 Krad)
7	TRIO (Temperature Remote I/O)	Includes 16 analog inputs for temperature or voltage measurement, 10 bit ADC and I <sup>2</sup> C interface.	TAS	APL	APL	Honeywell SSEC	Custom RICMOS4	~46K	84	ASIC in fabrication. EM parts due: 8/01

**NOTES:**

All ASICs are 1 Mrad except as noted

ASICs to be fabricated via the JPL Multifab Contract

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## Power Subsystem ASICs

	ASIC	Function	Slice	Designed By	Proc By	Fab By	Fab Line Type	Gate Count	Pin Count	Status
1	SCAH (Switch Control ASIC High)	Provides the floating current limit, overcurrent trip and MOSFET drive function for the power switch inside the PASM.	PSS PCS	Boeing	JPL	Honeywell SSEC	Mixed HX2040	<10K	60	On track for a CDR on 6/28/01. JPL is completing a worst case data base of the analog cells and will complete a formal worst case analysis by 5/31/01.
2	SCAL (Switch Control ASIC Low)	Provides the ground referenced command I/F and charge pump for the power switch inside the PASM.	PSS PCS	Boeing	JPL	Honeywell SSEC	Mixed HX2040	<10K	60	On track for a CDR on 6/28/01. JPL is completing a worst case data base of the analog cells and will complete a formal worst case analysis by 5/31/01.
3	PWMA (Pulse-Width Modulator ASIC)	Provides pulse width modulation control for a dual forward topology on the primary side of the Power Converter Module (PCM).	PCA	Boeing	JPL	Honeywell SSEC	Mixed HX2080	<10K	128	Completed fabrication of the first pass on 12/15/00. The part is fully functional with the exception of the autozero amplifier. Second pass specification for new MOSFET baseline has been started and detail design will start in June.
4	SRCA (Synchronous Rectifier ASIC)	Provides synchronous rectifier drive and output voltage and current sense on the secondary side of the PCM.	PCA	Boeing	JPL	Honeywell SSEC	Mixed HX2040	<10K	60	Completed fabrication of the first pass on 12/15/00. The part is fully functional with the exception of a POR timing issue. The second pass specification for new MOSFET baseline has been started and detail design will start in June.
5	AIA (Analog Interface ASIC)	Provides the system I2C bus interface and chops the signal across transformers for isolated interface with the CIA.	PSS PCS	JPL + SSEC	JPL	Honeywell SSEC	Custom HX2040	~20K	33 Sig 20 Grd	Tape out is scheduled for 7/1/01 and will be fabricated with the SCA. Analog cells will be complete by 4/23/01.
6	CIA (Command Interface ASIC)	Provides local command and control for the PCS and PSS including A/D conversion.	PSS PCS	JPL + SSEC	JPL	Honeywell SSEC	Mixed HX2300	87K gates + 1Kb RAM + 64Kb ROM	184 Sig 50 Grd	CDR is scheduled for 10/4/01. Analog cell layout, firmware and verilog code will be complete by 6/26/01.

NOTES:

All ASICs 1 Mrad unless otherwise noted

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## Future Status Updates

- Europa Orbiter Project Website:  
<http://www.jpl.nasa.gov/europaorbiter/index.htm>
- Presentations, status information, hardware specifications will be placed there as available



## Acronym List

ACS	Attitude Control Sensors	RTG	Radioisotope Thermoelectric Generator
AIA	Analog Interface ASIC	RWE	Reaction Wheel Electronics
CDH	Command and Data Handling	RWM	Reaction Wheel Motor
CIA	Command Interface ASIC	SCA	Switch Control ASIC
DIO	Digital I/O ASIC	SCRA	Synchronous Control Rectifier ASIC
IMU	Inertial Measurement Unit	SDST	Small Deep Space Transponder
MSIO	Mixed Signal I/O ASIC	SFC	System Flight Computer
NVM	Non Volatile Memory	SIA	System Interface Assembly
PASM	Power Activation and Switching Module	SIO	System I/O Board
PCA	Power Converter Assembly	SRU	Stellar Reference Unit
PCM	Power Converter Module	SSE	Sun Sensor Electronics
PCS	Power Control Slice	SSH	Sun Sensor Head
PSS	Power Switch Slice	TAS	TRIO Assembly Slice
PWMA	Pulse Width Modulator ASIC	TRIO	Temperature Remote I/O